REMARKS

By the present amendment, Applicants submit a substitute abstract to replace the original abstract. Applicants have amended claim 13 to more appropriately define the invention. Applicants have canceled claims 14-16 and 20-26, without prejudice or disclaimer of the subject matter thereof. Applicants have also added new claims 27-29 to protect additional aspects of the invention. Claims 13, 17-18, and 27-29 are pending, and claims 1-12 and 19 are withdrawn from consideration as directed to non-elected species.

In the Office Action, the Examiner objected to the abstract because the abstract "does [not] correspond to the claim language presented for examination." [1] The Examiner rejected claims 13-18 and 20-26 under 35 U.S.C. § 112, second paragraph, for lacking support in the specification, and rejected claims 13-18 and 20-26 under 35 U.S.C. § 103(a) as unpatentable over Sugibayashi (U.S. Patent No. 5,305,265).

It appears the Examiner has objected to the Abstract because it does not correspond to the claim language presented for examination. In this regard the Examiner cites M.P.E.P. § 608.01(b). Applicants respectfully disagree with the Examiner's grounds for objecting to the Abstract. M.P.E.P. § 608.01(b) clearly states that:

> A patent abstract is a concise statement of the **technical disclosure** of the patent and should include that which is new in the art to which the invention pertains. (emphasis added)

[1] In the objection to the abstract, the Examiner seems to have inadvertently omitted the word "not." Office Action, page 2.

Thus, M.P.E.P. § 608.01(b), which is in accord with 37 C.F.R. § 1.72, clearly requires that the Abstract be a concise statement of the **technical disclosure**, not the claim language.

Nevertheless, in response to the Examiner's objection, Applicants have submitted a substitute Abstract which conforms to the requirements of M.P.E.P. § 608.01(b). Support for the substitute Abstract is found in Applicants' Specification at, for example, page 14, line 27 - page 15, line 16.

The rejections of claims 14-16 and 20-26 are rendered moot in view of the cancellation thereof.

With regard to the rejection of claim 13 under 35 U.S.C. § 112, second paragraph, Applicants note that support for "an array selection circuit for generating said internal address signals on the basis of an external address signal and said selection control signal generated by said selection control circuit and outputting said internal address signals to said plurality of cell arrays to select ones of the cell arrays" of claim 13 may be found in the Specification at lines 6-12 of page 15 and lines 18-26 of page 37. Particularly, at lines 6-12 on page 15, array selection circuit 31 of Fig. 4 is described. At lines 21-26 on page 37, the Specification states that "[t]he basic configuration of [the fifth] embodiment is the same as that of the first embodiment," and that "FIG. 13 is a schematic block diagram of the fifth embodiment of semiconductor device according to the invention and corresponds to FIG. 4 illustrating the first embodiment." Therefore, the rejection of claim 13 under 35 U.S.C. § 112, second paragraph, should be withdrawn.

With regard to the rejection of claims 17 and 18 under 35 U.S.C. § 112, second paragraph, support for claims 17-18 can be found in the Specification at, for example, page 18, line 15 - page 19, line 4, and page 38, lines 10-22. Therefore, the rejection of claims 17-18 under 35 U.S.C. § 112, second paragraph, should be withdrawn.

Additionally, support for new claims 27-28 can be found in the Specification at, for example, page 18, line 15 - page 19, line 4, and page 20, lines 11-23. Support for new claim 29 can be found in the Specification at, for example, page 16, lines 8-10, page 16, line 26 - page 17, line 1.

Applicants respectfully traverse the rejection of claims 13 and 17-18 under 35 U.S.C. § 103(a), because a *prima facie* case of obviousness has not been established by the Examiner.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. M.P.E.P. §2143, 8th ed., Revision of May 2004.

Claim 13 recites a semiconductor device that includes, *inter alia*, "a selection control circuit for generating and outputting a selection control signal to be used for generating internal address signals; and an array selection circuit for generating said

internal address signals on the basis of an external address signal and said selection control signal generated by said selection control circuit and outputting said internal address signals to said plurality of cell arrays to select ones of the cell arrays."

The Examiner alleged that Sugibayashi's delay circuit 6 corresponds to Applicants' claimed "selection [control] circuit" and Sugibayashi's switching circuit 5 corresponds to Applicants' claimed "array selection circuit." Office Action, page 3. Applicants disagree.

Referring to Fig. 1 of Sugibayashi, "delay circuit 6 generates a selection signal YSW which is obtained . . . in response to a control signal DS from [ ] switching circuit 5. . . . The level setting for the control signal DS generated by the switching circuit 5 is carried out in response to the result of the function test in the wafer state." Sugibayashi, col. 3, ll. 40-55. Clearly, switching circuit 5 of Sugibayashi does not generate internal address signals on the basis of selection signal YSW generated by delay circuit 6. Thus, Sugibayashi's delay circuit 6 and switching circuit 5 cannot respectively correspond to Applicants' claimed "selection [control] circuit" and "array selection circuit."

Therefore, Sugibayashi fails to teach or suggest Applicants' claimed combination including, at least, "a selection control circuit for generating and outputting a selection control signal to be used for generating internal address signals; and an array selection circuit for generating said internal address signals on the basis of an external address signal and said selection control signal generated by said selection control circuit and outputting said internal address signals to said plurality of cell arrays to select ones of

the cell arrays," as recited in claim 13. Accordingly, claim 13 is patentable over Sugibayashi.

Claims 17-18 and 27-29 depend from claim 13 and are also patentable at least because of their dependence from an allowable base claim.

In view of the foregoing, Applicants respectfully request reconsideration of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account no. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: February 16, 2005

By: _____
Qingyu Yin*

*With limited recognition under 37 C.F.R. § 10.9(b).

Attachment:

Substitute Abstract

A semiconductor device includes a plurality of cell arrays, a selection control circuit to generate and to output a selection control signal to be used to generate internal address signals. An array selection circuit generates the internal address signals on the basis of an external address signal and the selection control signal generated by the selection control circuit. The array selection circuit outputs the internal address signals to the plurality of cell arrays to select ones of the cell arrays.